

DETAILED ACTION

This Office Action is in response to Dismissal of Appeal ordered by the Board of Patent Appeals and Interferences on 10/24/2008, as requested by Applicant's on filed paper requesting to withdrawn the appeal filed on 10/8/2008.

The Voluntary Amendment filed on 10/8/2008 has been entered and considered by the Examiner.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 4/28/2009 was filed after the is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Allowable Subject Matter

2. Claims 1-20 are allowed.
3. The following is an examiner's statement of reasons for allowance:

Independent Claim 1, is allowable over the prior art of record since the cited references, in particular Luo (US 6,111,467), Beauducel et al (US 4, 352,070), Dingwall et al. (US 5,036,219) taken alone or in combination do not teach or suggest a sample and hold circuit comprising *an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is substantially limited to said offset voltage, wherein parasitic drain and source diodes (D0, D1) of an NMOS switch are coupled to a voltage that is more negative than an input signal of said NMOS switch in a sample mode, wherein said parasitic drain and source diodes of said NMOS switch are coupled to an output of said amplifier in a hold mode. wherein parasitic drain and source diodes (D2, D3) of a PMOS switch are*

coupled to a voltage that is more positive than an input signal of said PMOS switch in a sample mode, and wherein said parasitic drain and source diodes of said PMOS switch are coupled to an output of said amplifier in a bold mode, in combination with the other limitations in the claim.

Independent Claim 8, is allowable over the prior art of record since the cited references, in particular Luo (US 6,111,467), Beauducel et al (US 4, 352,070), Dingwall et al. (US 5,036,219) taken alone or in combination do not teach or suggest a method comprising *substantially limiting leakage current in parasitic drain and source diodes of an NMOS switch by coupling said parasitic drain and source diodes of said NMOS switch to a voltage that is more negative than an input signal of said NMOS switch in a sample mode and coupling said parasitic drain and source diodes of said NMOS switch to an output of said amplifier in a bold mode, and limiting leakage current in parasitic drain and source diodes of a PMOS switch by coupling said parasitic drain and source diodes of said PMOS switch to a voltage that is more positive than an input signal of said PMOS switch in a sample mode and by coupling said parasitic drain and source diodes of said PMOS switch to an output of said amplifier in a bold mode*, in combination with the other limitations in the claim.

Independent Claim 14, is allowable over the prior art of record since the cited references, in particular Luo (US 6,111,467), Beauducel et al (US 4, 352,070), Briskin (US 6,721,117), taken alone or in combination do not teach or suggest disk drive comprising *an amplifier connected to said node, wherein said amplifier has an offset voltage and wherein a voltage drop across at least one of said input and output switches is limited to said offset voltage, wherein parasitic drain and source diodes (D0, D1) of an NMOS switch are coupled to a voltage that is more negative than an input signal of said NMOS switch in a sample mode, wherein said parasitic drain and source diodes of said NMOS switch are coupled to an output of said amplifier in a bold mode, wherein parasitic drain and source diodes (D2, D3) of a PMOS switch are coupled to a voltage that is more positive than an input signal of said PMOS switch in a sample mode, and wherein said parasitic drain and source diodes of*

said PMOS switch are coupled to an output of said amplifier in a bold mode, in combination with the other limitations in the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Otake (US 6,909,249); Hickling et al. (US 6,323,696); Otake (US 7,034,607); Kiriaki et al. (US 6,262,677); Birdsall et al. (US 6,028,459); Miki et al. (US 5,341,037); Linder (US 5,313,113); Hsieh (US 5,838,175); Cosand et al. (US 4,370,572); Aranovsky (US 5,331,478); Kawai (US 6,522,491); Rakers et al. (US 5,572,154).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DISMERY E. MERCEDES whose telephone number is (571) 272-7558. The examiner can normally be reached on Monday - Friday, from 7:00am - 3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Thi Nguyen can be reached on 571-272-7579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dismery E. Mercedes/
Primary Examiner, Art Unit 2627